RTDS Technologies

the world standard for real time digital power system simulation

HVDC and FACTS

HVDC and FACTS devices are among many critical technologies for ensuring and enhancing the controllability, reliability, and safety of modern power networks. The RTDS Simulator was originally developed to model HVDC schemes, and over the last two decades the Simulator has revolutionized the testing process for HVDC controls. Today, it is the ideal tool for the simulation and testing of HVDC and FACTS devices. RSCAD includes a wide variety of sample cases relating to HVDC and FACTS applications, including MMC (Modular Multilevel Converter) HVDC, SVC MMC, and LCC HVDC schemes, among others.


Photo: ABB

All of the major manufacturers use the RTDS Simulator to test their HVDC controls during Factory Systems Testing. Systems successfully tested include LCC- and VSC-based HVDC, modular multi-level converters, network and industrial SVCs, STATCOM, TCSC, DVR, UPFC, and more.

Furthermore, many electrical utilities around the world have purchased an RTDS Simulator to connect to replica controls for HVDC and FACTS projects. In these cases, a slightly simplified copy of the controls are delivered to site along with an RTDS Simulator to represent the power system. These "replica Simulators" are then interfaced with the controls and are generally used to investigate proposed network changes and control modifications, to test scheme upgrades and refurbishment, and to train utility personnel on scheme theory and operation. A few notable utility projects are listed here for reference.

The RTDS Simulator is used by utilities worldwide for HVDC and FACTS projects

Rio Madeira HVDC Project: Operador Nacional do Sistema Elétrico, a Brazilian utility, is responsible for the coordination and control of the Rio Madeira HVDC link. At 2,375 km long, it is the longest transmission link in the world at the time of writing. The controls for this project were tested exclusively on the RTDS Simulator.

Trans Bay Cable: This 85 km submarine HVDC cable transfers energy from the City of Pittsburg to the City of San Francisco. This was the world's first ever HVDC project to use an MMC system, and was tested using the RTDS Simulator.

North-East Agra UHVDC Project: Power Grid Corporation of India is responsible for the world's first ever multi-terminal UHVDC transmission link. The link includes four terminals in three converter stations with a total converter capacity of over 8,000 MW—the largest HVDC transmission system ever built. This project was tested using the RTDS Simulator.

Learn more about these and other HVDC and FACTS projects involving the RTDS Simulator at **www.rtds.com/applications/hvdc-and-facts.**

The small timestep library of RSCAD contains an extensive selection of HVDC- and FACTS-related components. RSCAD's small timestep subnetworks operate with timesteps in the range of 1-4 µs and can be interfaced to large scale simulations operating with timesteps in the order of 25-50 µs. A key feature of these subnetworks is that the circuit and valve topology is user configurable. Two- and three-level converters can be freely configured to provide crow-bar circuits, etc. for PWM switching at greater than 2 kHz. A low-loss, fixed topology two-level converter is also available for operation at PWM switching frequencies in the range of 20 kHz. Multiple VSC subnetworks can be linked together by traveling wave transmission lines or cables to create entire sytems running with timesteps <4 µs.

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A wide variety of HVDC and FACTS models are available in the RSCAD model library

The development team at RTDS Technologies is always working on improving existing models and adding new models to RSCAD. Currently, the RSCAD model library includes the following:

LCC Models: RSCAD contains both six- and twelve-pulse LCC valve group models. The models support a broad range of valve faults, both between internal nodes and also to external nodes. These can be easily configured to represent UHVDC (i.e. with several series groups) and allow faults to points both internal and external to the converter. The improved firing algorithm is used to allow the converters to represent a continually variable firing instant with an accuracy of 1 µs.

VSC Models: Two- and three-level converter models, including point-to-point and back-to-back schemes, are available. RSCAD also includes several models for Modular Multilevel Converters (MMC). MMCs offer many advantages over conventional thyristor-based schemes and are increasingly popular for HVDC and FACTS applications. The MMC models available for the RTDS Simulator are described in the section below.

Sub-step VSC Models: These new two- and three-level VSC models operate in the sub-small-timestep (or "sub-step") region, meaning that they can run at a timestep as small as 1/3 of the small timestep. With up to 3 sub-steps in a regular small timestep, these components reduce switching losses by approximately 50% and allows switching at higher frequencies.

Firing Pulse and Ramp Generators: High resolution firing pulse words can be produced in the VSC small time-step code through use of VSC firing pulse generation blocks available in the library. They can also be brought into the simulation directly from a GTDI digital input card.

Small timestep frequency-dependent T-Line: This 8– or 12-conductor frequency dependent phase domain travelling wave transmission line model runs at 2.5-3.75 µs on the GTFPGA Unit and avoids the use of long interface Bergeron lines.

The controls for the Rio Madeira HVDC system—the longest transmission link in the world—were tested on the RTDS Simulator.

Photo: ABB

Modular Multilevel Converters

The RTDS Simulator features two main types of MMC models: processor-based MMC models, which are executed on NovaCor™ hardware or processor cards within the RTDS Simulator cubicle, and FPGA-based models, which are executed on a dedicated piece of hardware called the GTFPGA Unit.

Unified Model (FPGA-based): The Unified Model (U5) can be used to represent up to 6 valve legs on one GTFPGA Unit. Each valve leg can include up to 768 submodules. Both half and full bridge configurations are supported. Normal firing states (blocked, positive inserted, negative inserted, and bypassed) are considered. Internal faults can be simulated, but not at the individual IGBT level. U5 supports the addition of a damping submodule.

Generic Model (FPGA-based): The Generic Model (GM) can be used to represent up to 2 valve legs on one GTFPGA Unit. Each valve leg can include up to 1024 submodules. Half, full, and mixed (half/full) bridge configurations are supported. All possible IGBT firing states are considered. The GM supports individual IGBT firing, individual submodule capacitances, customized topologies, internal valve to ground faults, and the addition of a damping submodule.

MMC5 (processor-based): The MMC5 component is designed for the testing of high level controls and system performance. Three valve legs can be simulated on one PB5 processor. Each valve leg can have up to 640 submodules. Both full and half bridge configurations are supported. Ideal capacitor voltage balancing is provided internally by the model. At the end of each small timestep, all submodules arrive at the same capacitor voltage.

CHAINV5 (processor-based): The CHAINV5 is a processor-based model that supports individual submodule firing pulse input, and can be used to test detailed firing pulse controls. CHAINV5 can model 40 submodules per valve for a full bridge configuration, or 56 submodules per valve for a half bridge configuration. The simulation of internal faults is not permitted.